FIG. 1

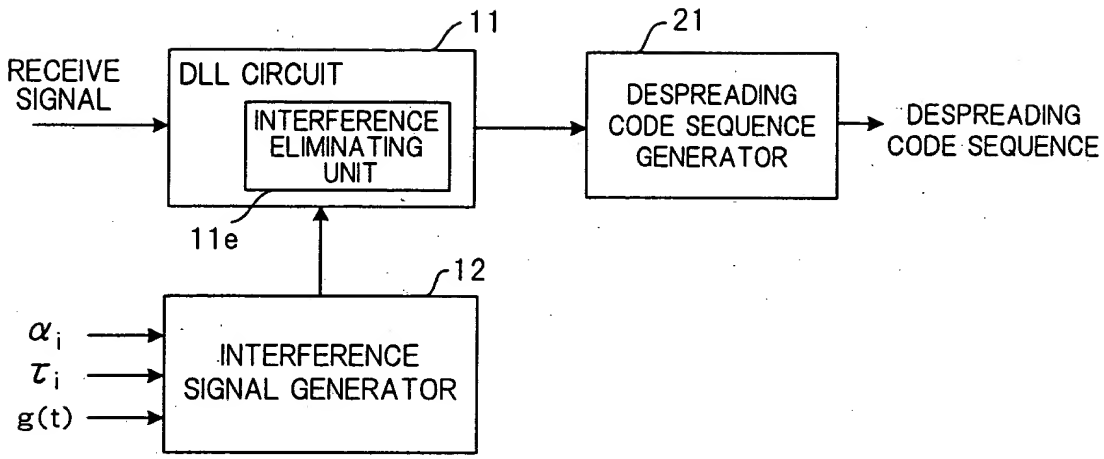
11
21
RECEIVE SIGNAL
DLL CIRCUIT
INTERFERENCE ELIMINATING UNIT
DESPREADING CODE SEQUENCE GENERATOR
DESPREADING CODE SEQUENCE
11e
12
α_i
τ_i
g(t)
INTERFERENCE SIGNAL GENERATOR

FIG. 2

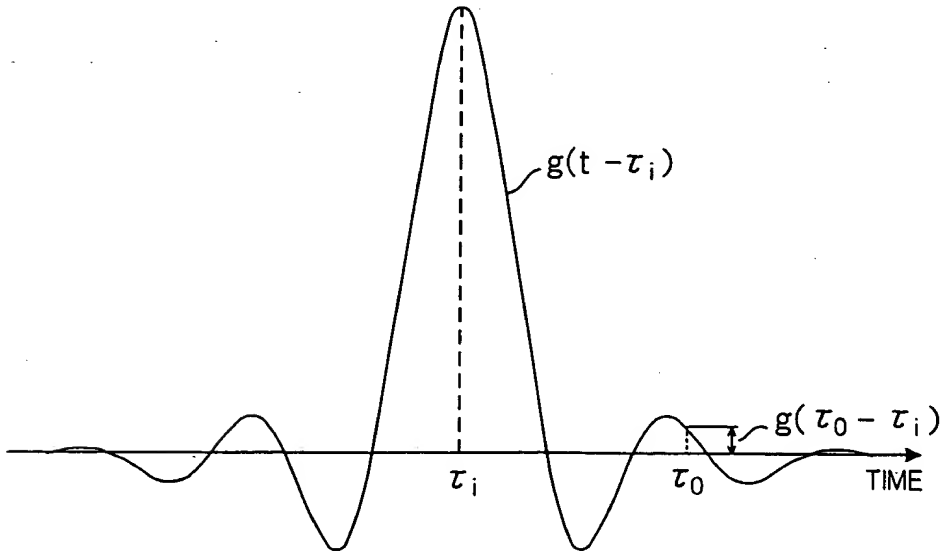
$g(t-\tau_i)$
$g(\tau_0-\tau_i)$
τ_i
τ_0
TIME

FIG. 3

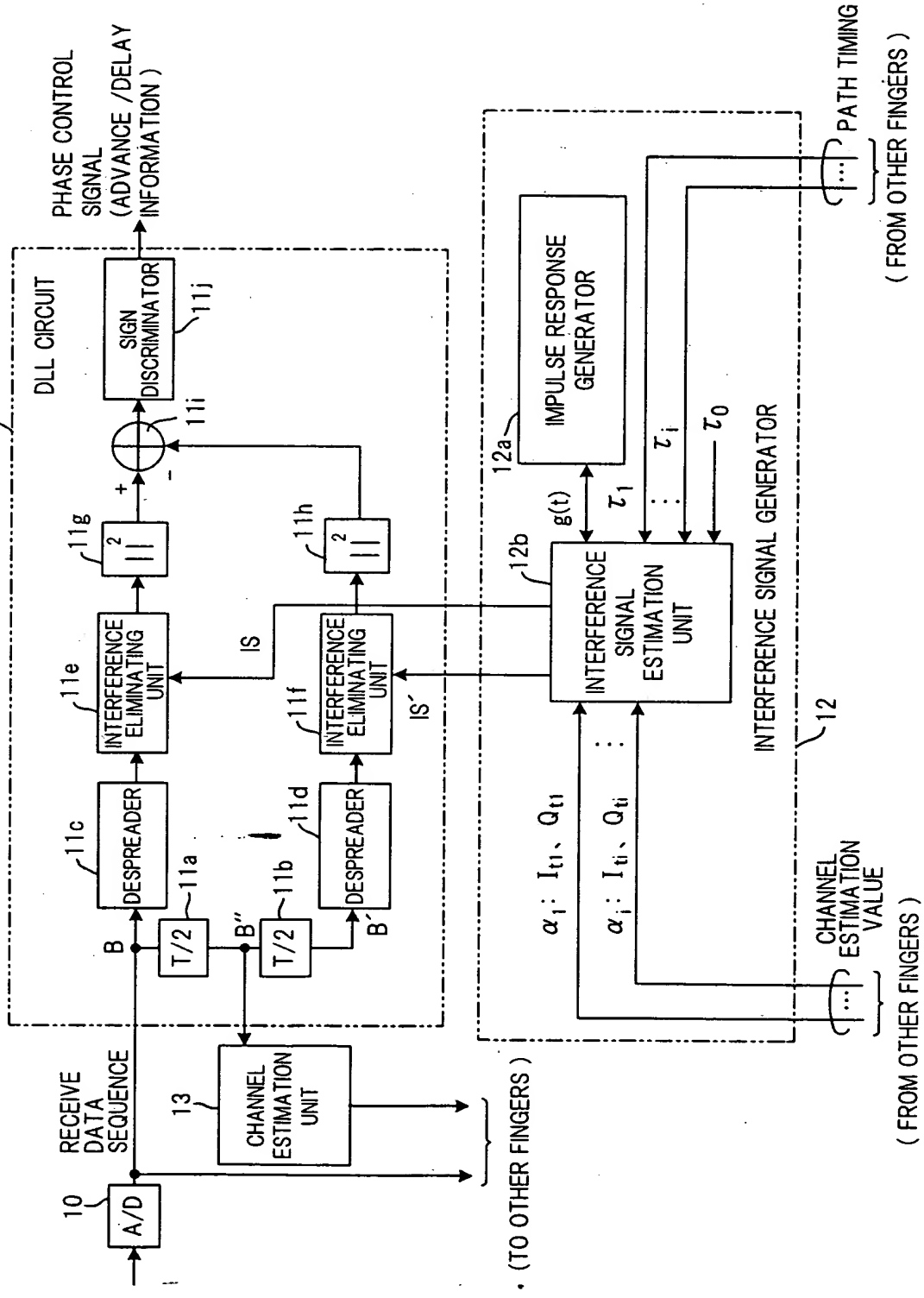
PHASE CONTROL SIGNAL (ADVANCE /DELAY INFORMATION)
11
DLL CIRCUIT
SIGN DISCRIMINATOR
11j
11i
11g
11h
INTERFERENCE ELIMINATING UNIT
11e
11f
IS
IS'
DESPREADER
11c
11d
B
B'
B''
T/2
11a
11b
RECEIVE DATA SEQUENCE
10
A/D
13
CHANNEL ESTIMATION UNIT
(TO OTHER FINGERS)
IMPULSE RESPONSE GENERATOR
12a
g(t)
12b
INTERFERENCE SIGNAL ESTIMATION UNIT
INTERFERENCE SIGNAL GENERATOR
12
PATH TIMING
(FROM OTHER FINGERS)
CHANNEL ESTIMATION VALUE
(FROM OTHER FINGERS)

FIG. 4

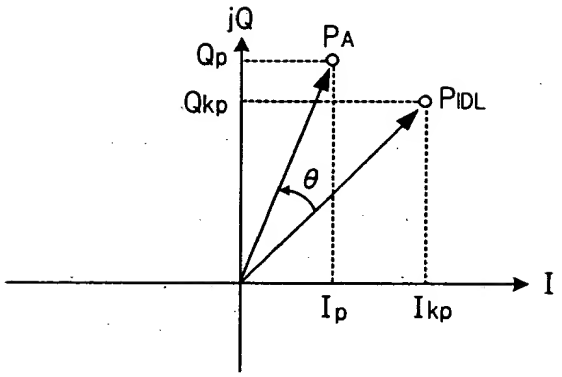
jQ
Qp
PA
Qkp
PIDL
θ
I
Ip
Ikp

FIG. 5

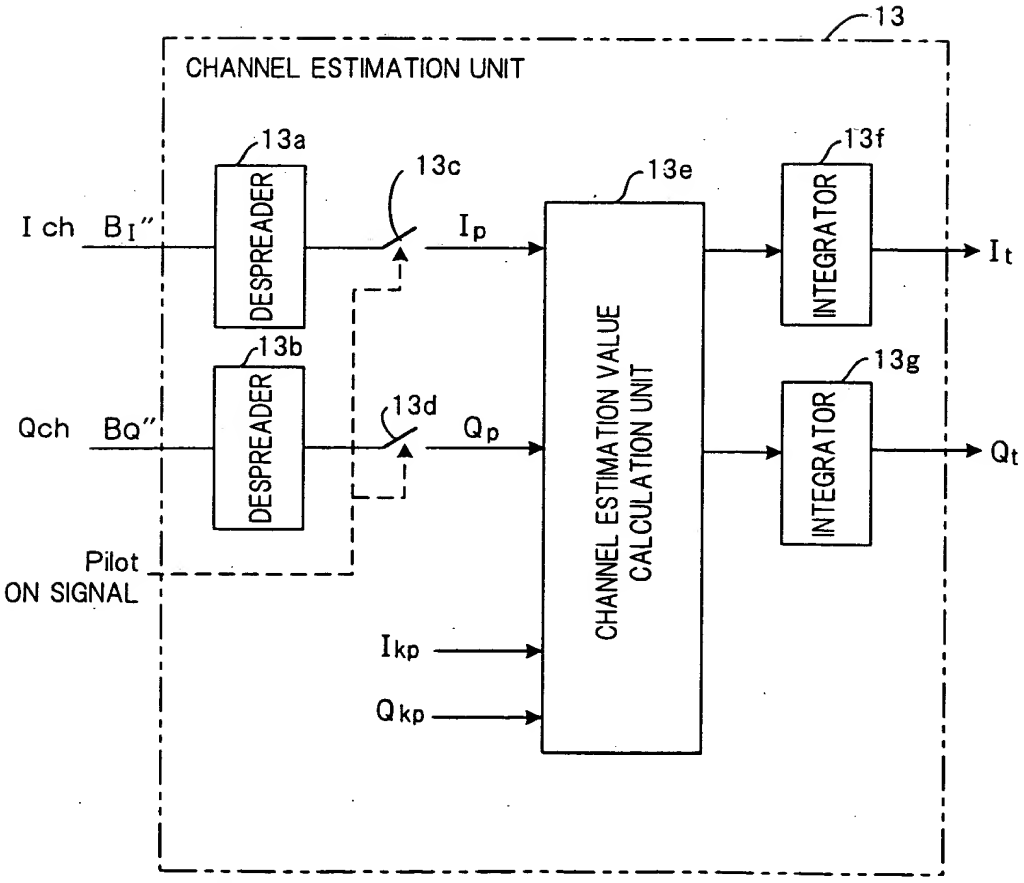
13
CHANNEL ESTIMATION UNIT
13a
DESPREADER
13c
13e
13f
INTEGRATOR
I ch
BI"
Ip
It
13b
DESPREADER
13d
13g
INTEGRATOR
Qch
BQ"
Qp
Qt
Pilot
ON SIGNAL
CHANNEL ESTIMATION VALUE CALCULATION UNIT
Ikp
Qkp

FIG. 6

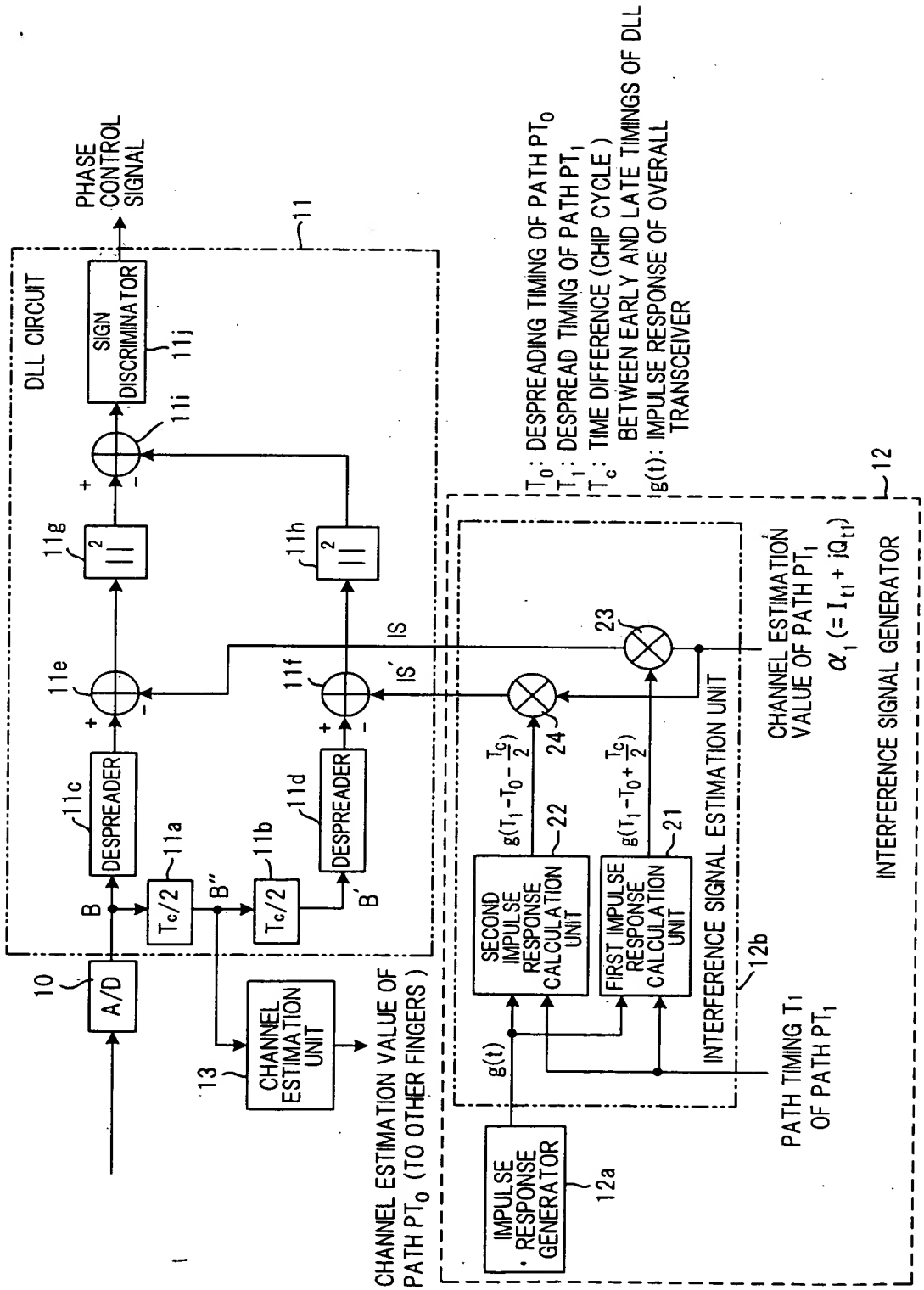
PHASE CONTROL SIGNAL
DLL CIRCUIT
11
SIGN DISCRIMINATOR
11j
11i
11g
11h
11e
11f
IS
IS'
DESPREADER
11c
DESPREADER
11d
Tc/2
11a
Tc/2
11b
B
B''
B'
10
A/D
13
CHANNEL ESTIMATION UNIT
CHANNEL ESTIMATION VALUE OF PATH PT0 (TO OTHER FINGERS)
T0: DESPREADING TIMING OF PATH PT0
T1: DESPREAD TIMING OF PATH PT1
Tc: TIME DIFFERENCE (CHIP CYCLE) BETWEEN EARLY AND LATE TIMINGS OF DLL
g(t): IMPULSE RESPONSE OF OVERALL TRANSCEIVER
12
23
24
22
21
SECOND IMPULSE RESPONSE CALCULATION UNIT
FIRST IMPULSE RESPONSE CALCULATION UNIT
CHANNEL ESTIMATION VALUE OF PATH PT1
α1 (= It1 + jQt1)
INTERFERENCE SIGNAL ESTIMATION UNIT
12b
INTERFERENCE SIGNAL GENERATOR
g(t)
PATH TIMING T1 OF PATH PT1
IMPULSE RESPONSE GENERATOR
12a

FIG. 7

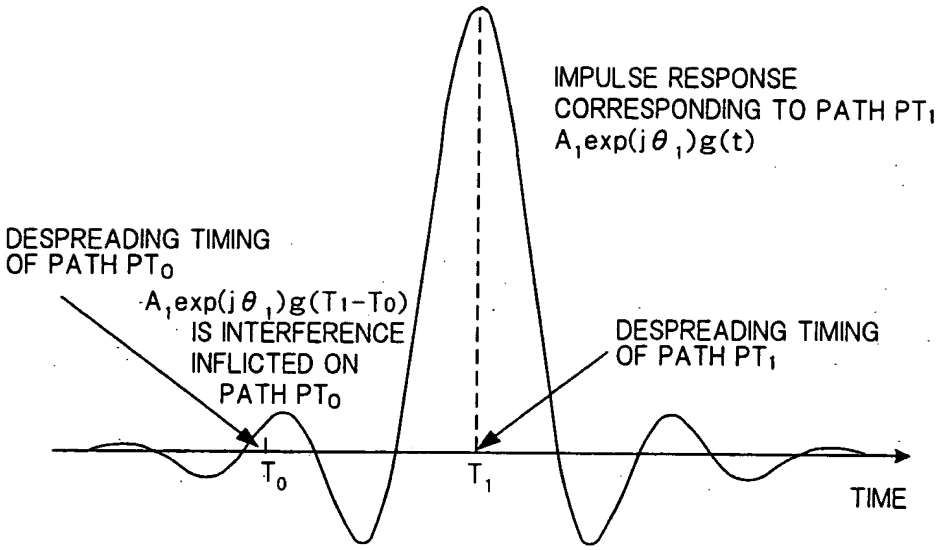
IMPULSE RESPONSE
CORRESPONDING TO PATH PT1
A1exp(jθ1)g(t)
DESPREADING TIMING
OF PATH PT0
A1exp(jθ1)g(T1-T0)
IS INTERFERENCE
INFLICTED ON
PATH PT0
DESPREADING TIMING
OF PATH PT1
T0
T1
TIME

FIG. 8

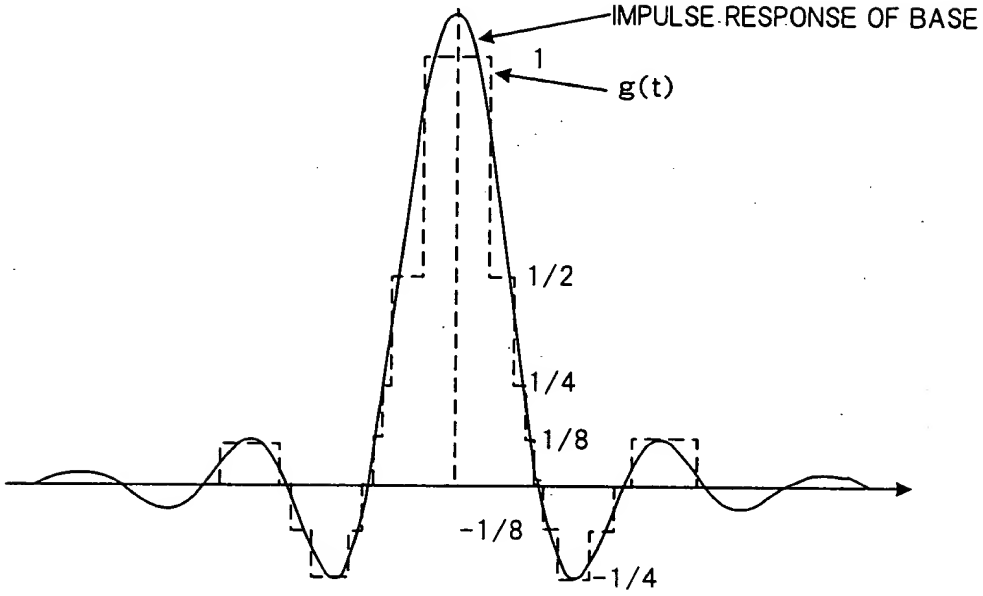
IMPULSE RESPONSE OF BASE
1
g(t)
1/2
1/4
1/8
-1/8
-1/4

FIG. 9

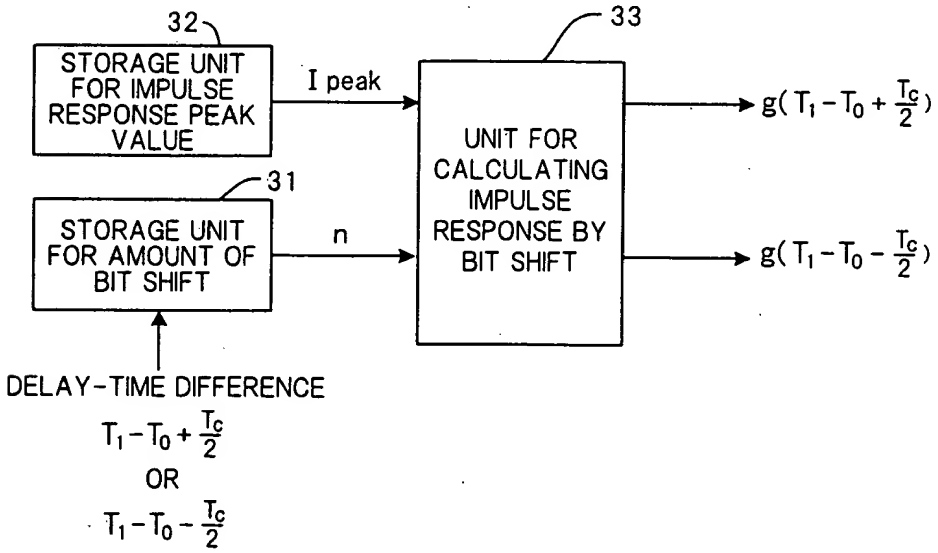
32
STORAGE UNIT FOR IMPULSE RESPONSE PEAK VALUE
I peak
33
UNIT FOR CALCULATING IMPULSE RESPONSE BY BIT SHIFT
$g(T_1-T_0+\frac{T_c}{2})$
31
STORAGE UNIT FOR AMOUNT OF BIT SHIFT
n
$g(T_1-T_0-\frac{T_c}{2})$
DELAY-TIME DIFFERENCE
$T_1-T_0+\frac{T_c}{2}$
OR
$T_1-T_0-\frac{T_c}{2}$

FIG. 10

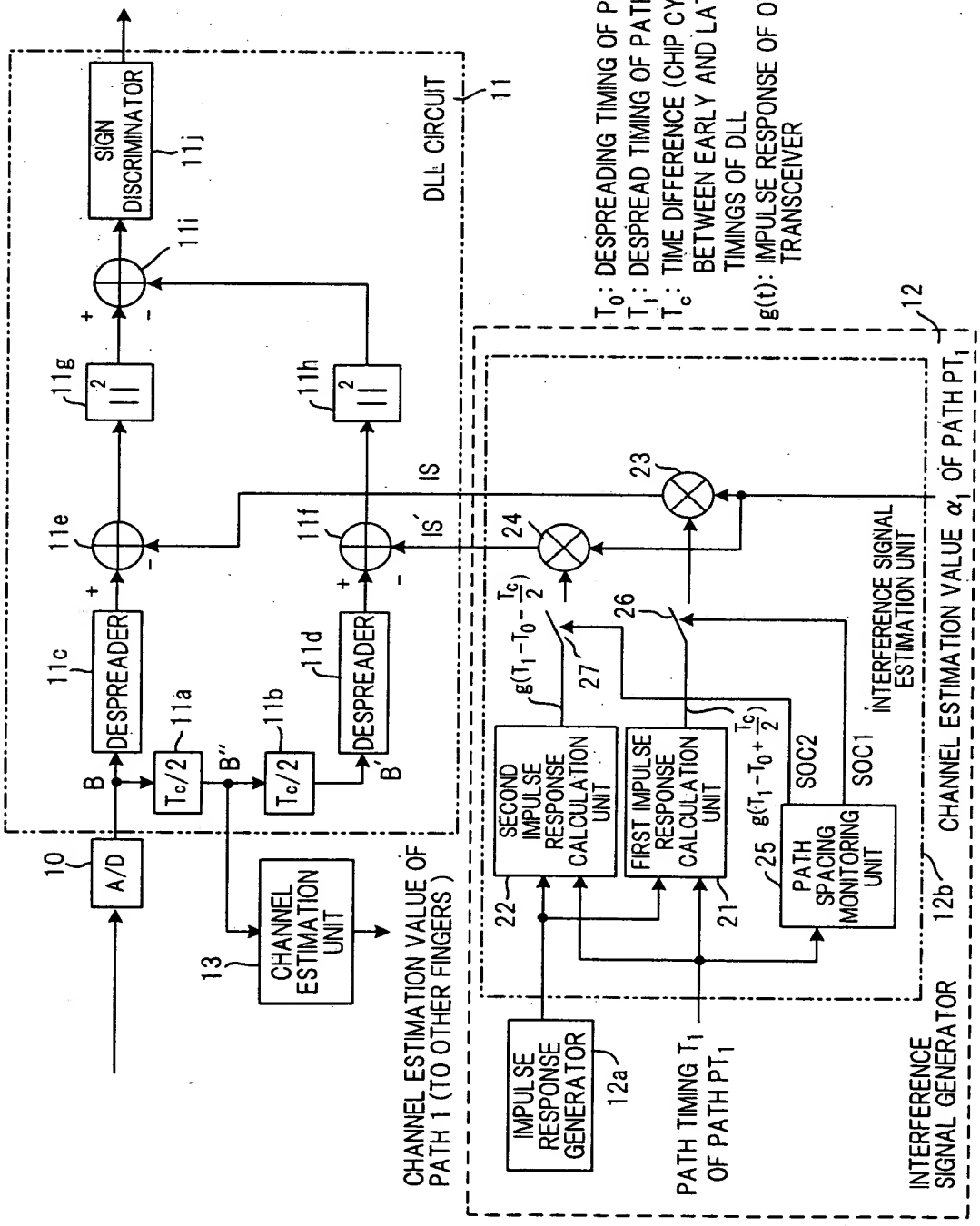
A/D
10
DESPREADER
11c
DESPREADER
11d
Tc/2
11a
Tc/2
11b
B
B''
B'
DLL CIRCUIT
11
SIGN DISCRIMINATOR
11j
11i
11g
11h
11e
11f
IS
IS'
CHANNEL ESTIMATION UNIT
13
CHANNEL ESTIMATION VALUE OF PATH 1 (TO OTHER FINGERS)
IMPULSE RESPONSE GENERATOR
12a
SECOND IMPULSE RESPONSE CALCULATION UNIT
FIRST IMPULSE RESPONSE CALCULATION UNIT
PATH SPACING MONITORING UNIT
SOC1
SOC2
INTERFERENCE SIGNAL ESTIMATION UNIT
12b
CHANNEL ESTIMATION VALUE α_1 OF PATH PT_1
12
PATH TIMING T_1 OF PATH PT_1
INTERFERENCE SIGNAL GENERATOR
T_0: DESPREADING TIMING OF PATH PT_0
T_1: DESPREAD TIMING OF PATH PT_1
T_c: TIME DIFFERENCE (CHIP CYCLE) BETWEEN EARLY AND LATE TIMINGS OF DLL
g(t): IMPULSE RESPONSE OF OVERALL TRANSCEIVER

FIG. 11

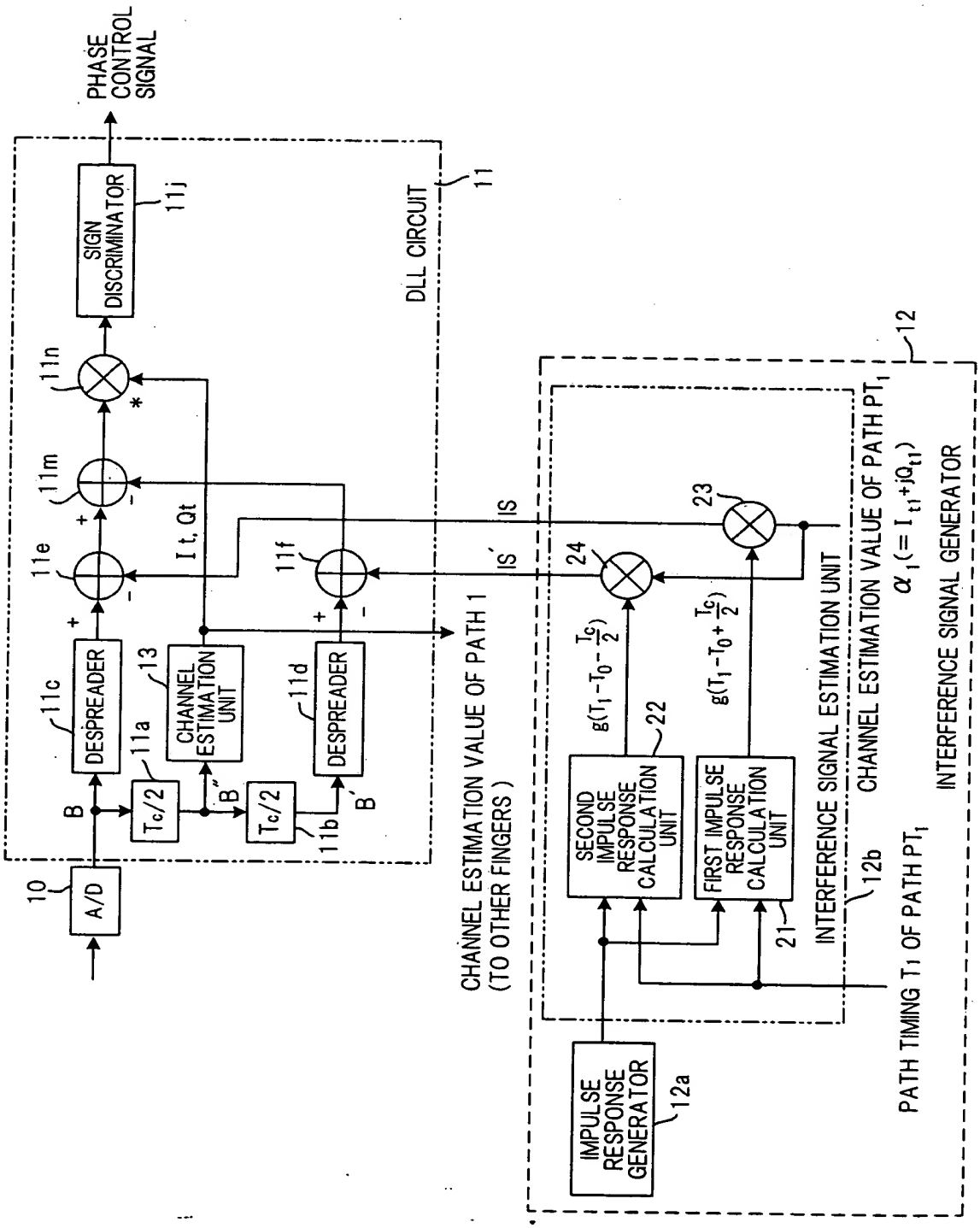
PHASE CONTROL SIGNAL
SIGN DISCRIMINATOR
11j
DLL CIRCUIT
11
11n
11m
11e
11f
I t, Qt
IS
IS'
DESPREADER
11c
11a
13
CHANNEL ESTIMATION UNIT
11d
DESPREADER
B
B''
B'
Tc/2
Tc/2
11b
10
A/D
CHANNEL ESTIMATION VALUE OF PATH 1 (TO OTHER FINGERS)
12
CHANNEL ESTIMATION VALUE OF PATH PT1
α1(= It1+jQt1)
INTERFERENCE SIGNAL GENERATOR
INTERFERENCE SIGNAL ESTIMATION UNIT
12b
21
SECOND IMPULSE RESPONSE CALCULATION UNIT
22
FIRST IMPULSE RESPONSE CALCULATION UNIT
23
24
g(T1-T0-Tc/2)
g(T1-T0+Tc/2)
IMPULSE RESPONSE GENERATOR
12a
PATH TIMING T1 OF PATH PT1

FIG. 12 PRIOR ART

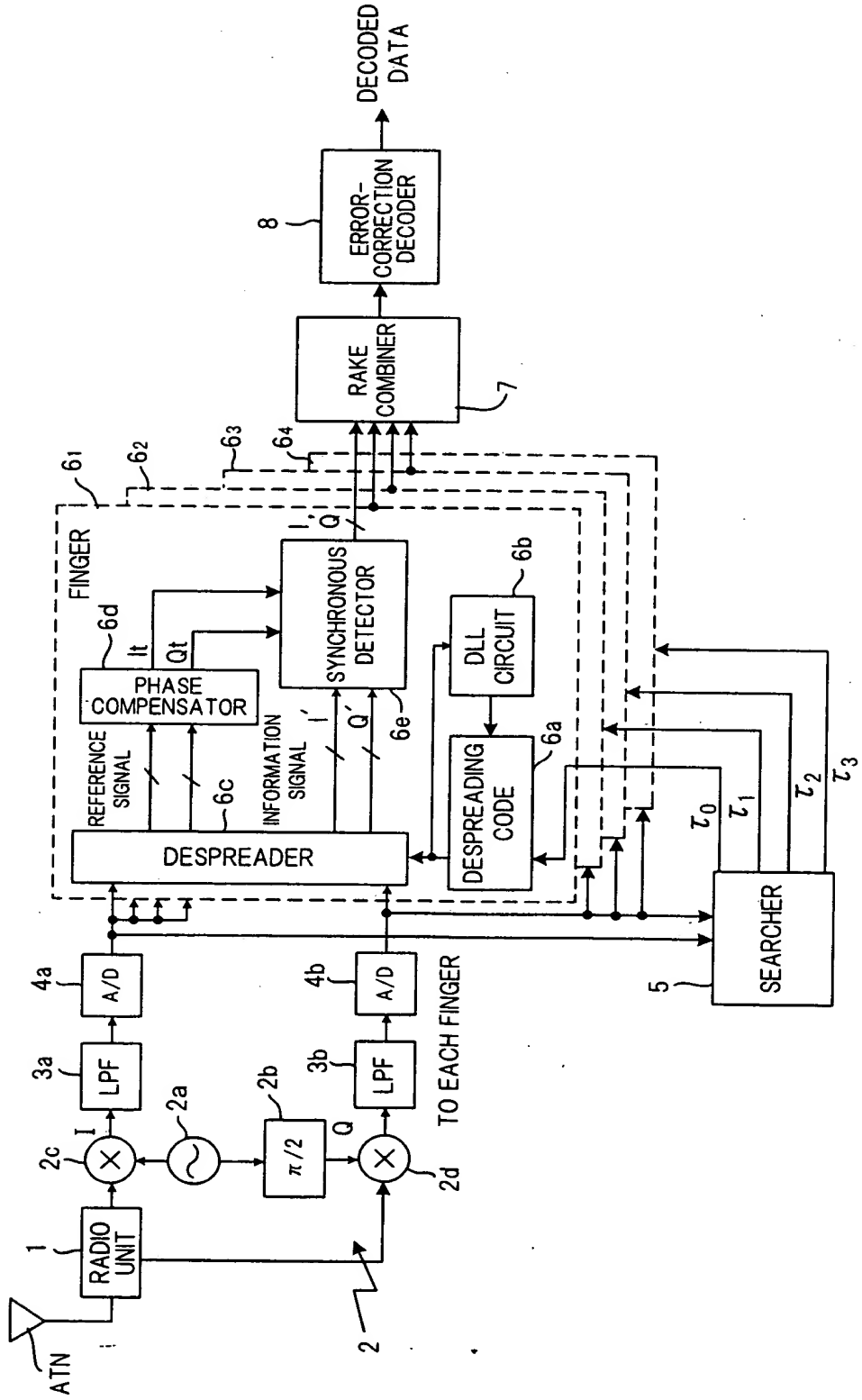

FIG. 13 PRIOR ART

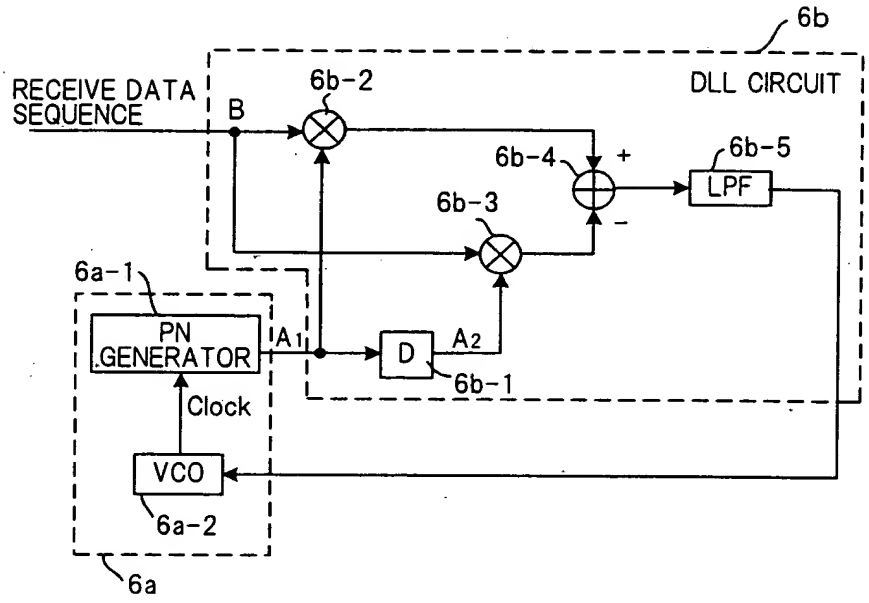

FIG. 14 PRIOR ART

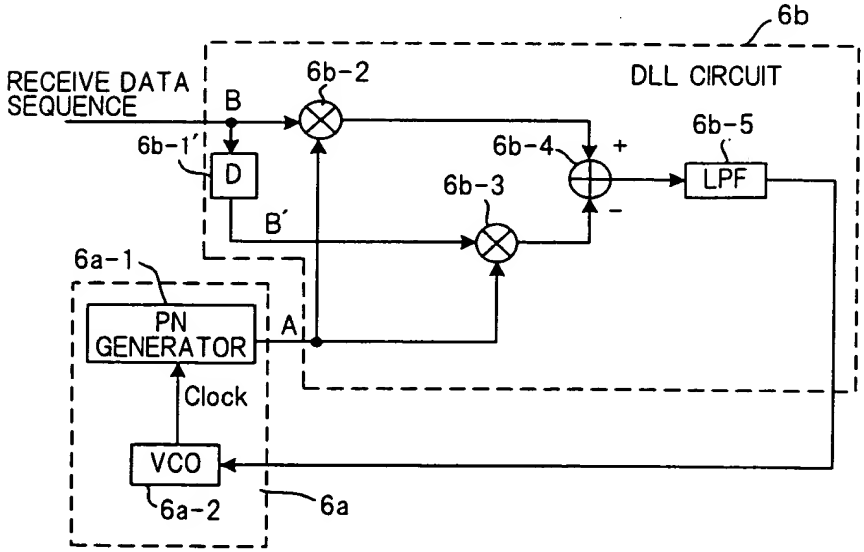

FIG. 15A PRIOR ART

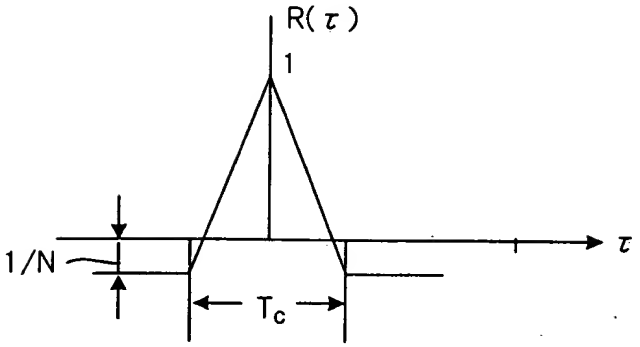

FIG. 15B PRIOR ART

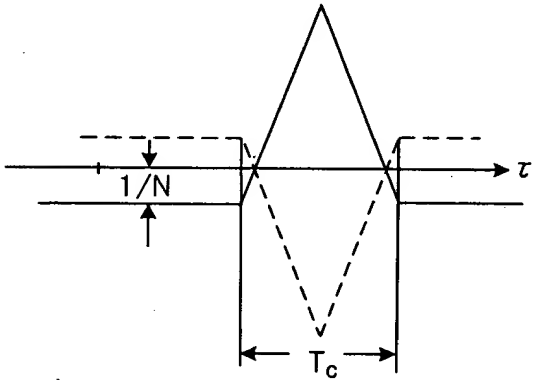

FIG. 15C PRIOR ART

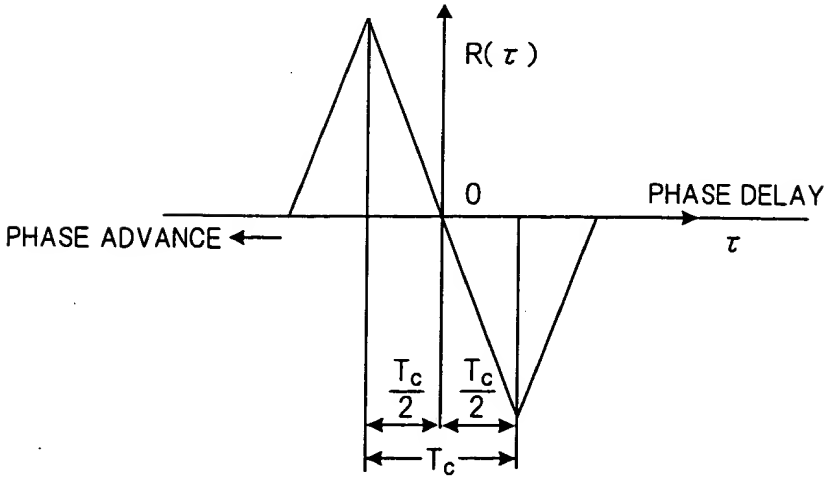

FIG. 16 PRIOR ART

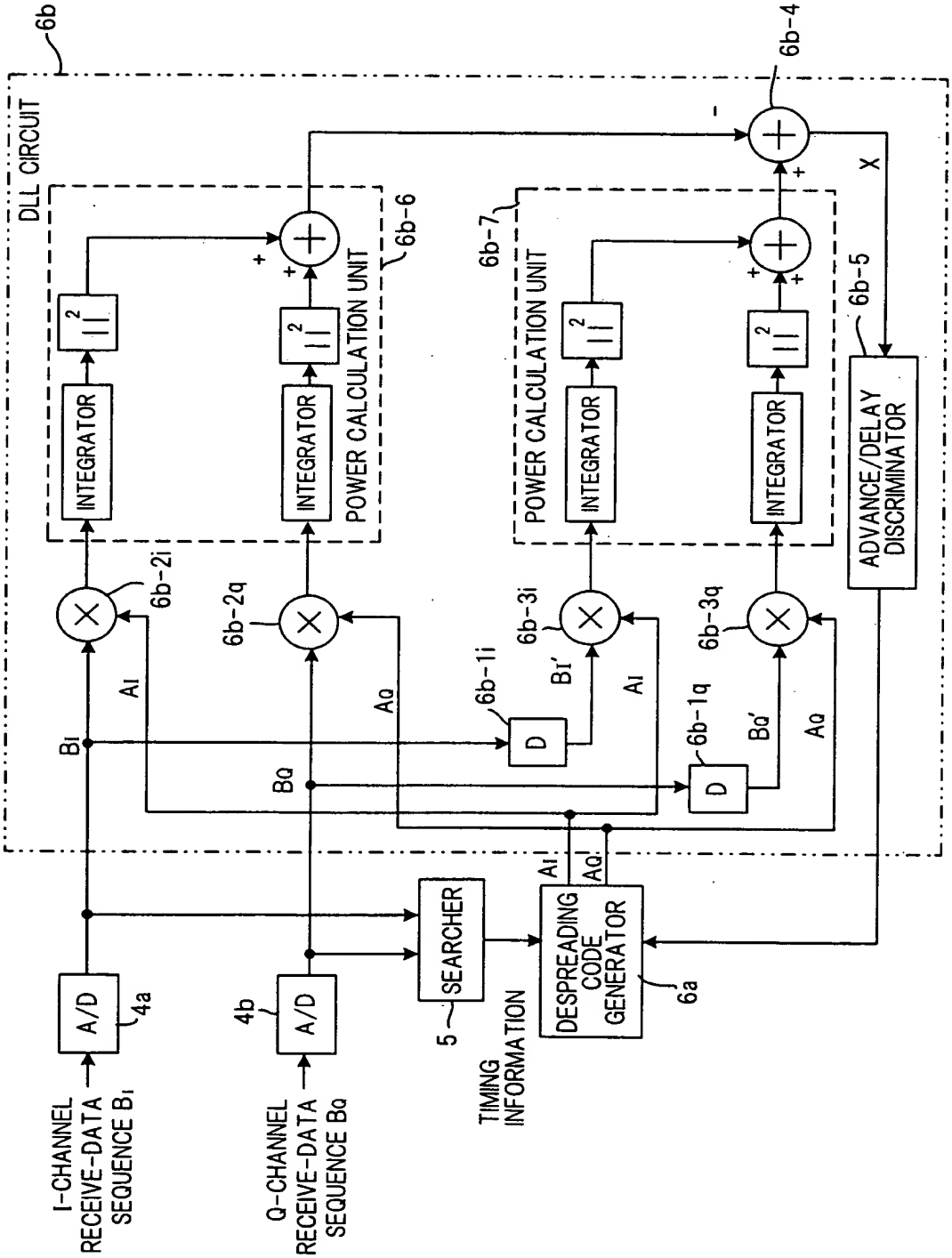

FIG. 17 PRIOR ART

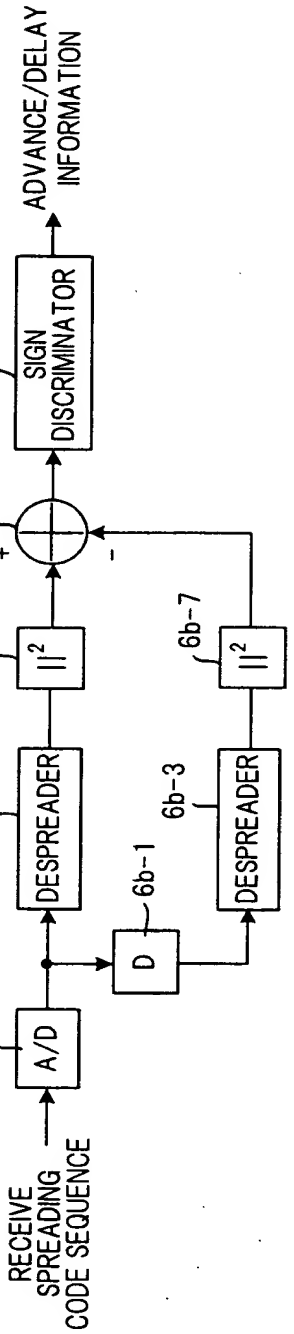

FIG. 18 PRIOR ART

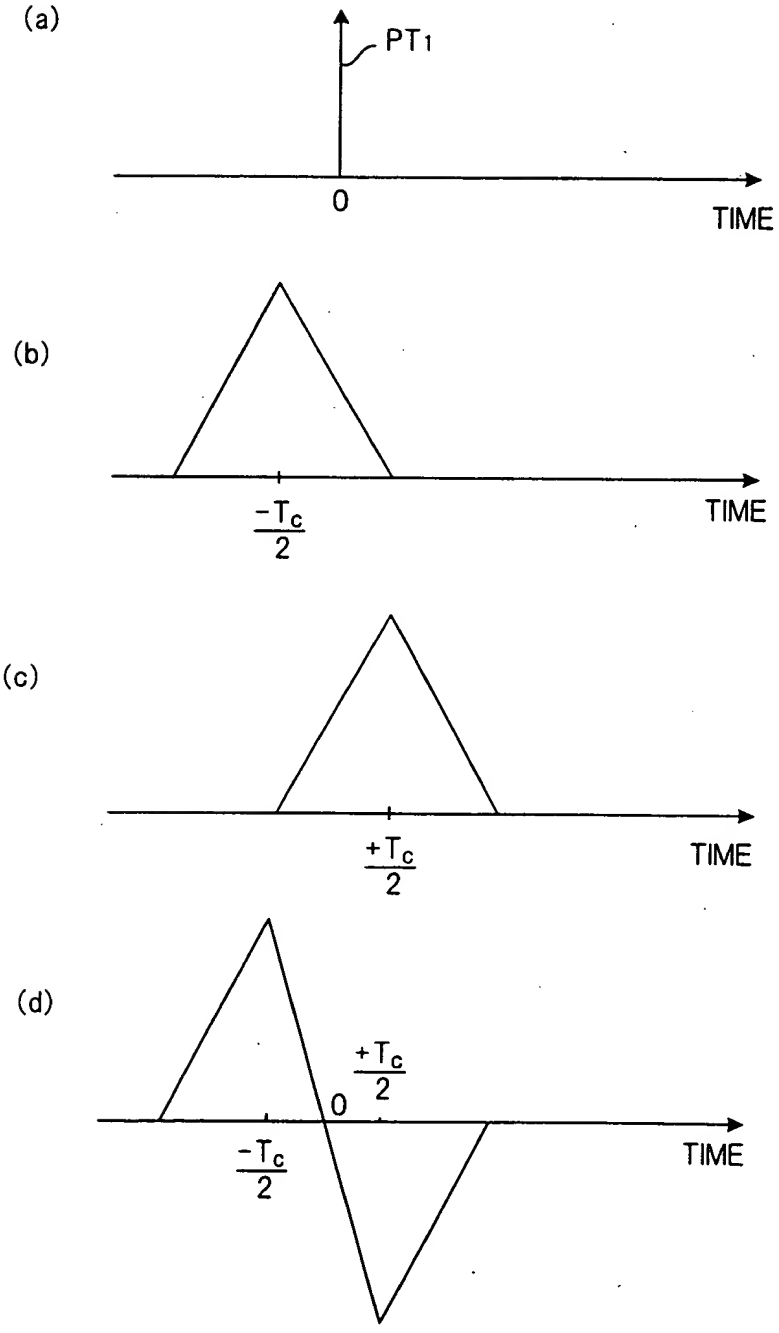

FIG. 19 PRIOR ART